MICROCONTROLLER BASED ISOLATED BOOST DC-DC CONVERTER

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Abstract

ZVS-PWM isolated boost DC-DC converter. It takes the supply from fuel cell battery at the input side compared to the previous full bridge converter, This half bridge converter to produce the same efficiency. The advantages of the paper is to reduce the number of devices and the mean time to reduce the losses, correspondingly to reduce the space and design cost. The system is simple and easy to operate the entire circle without more additional devices. It is used for medium and high power application. Zero voltage switching is applied in all the inverters. It is achieved the power flow in either direction. The circuit is compact packaging and reduce the losses. The simulation results are of closely agree with the theoretical approach a high efficiency achieved by using a minimal number of electronic devices working in the soft switching mode. It is operated at the frequency of 55 khz.

Terms DC-DC converter, soft switching, bi-directional power flow, conduction, losses, zero current switching and zero voltage switching.

I. INTRODUCTION

The necessity of high power isolated bidirectional DC-DC converter can be utilized in wide application from uninterrupted power supplies, battery charging and discharging systems. Most of the DC-DC converters are low power or unidirectional cannot meet the requirements of the above applications.

Nowadays some high power DC-DC converters with soft switching operation has been introduced in the literature [3]-[6]. These converters reduces the switching losses, improved EMI and increased efficiency. These converters are not absolutely achieve the high power density, high reliability and low cost. The circuit has not used the extra devices so there is no bulky and costly implementation. The paper introduces the high power application of isolated boost DC-DC converter. A dual half bridge converter is developed to achieve high power rating. Zero voltage switching is applied in either direction of power flow without using voltage clamping circuit. The circuit is required minimum number of devices. The input DC voltage is 12V battery to desire higher voltage (normally 150V-300V) for fuel cell to start. The DC-DC converters recharges the battery from the fuel cell or regenerative braking. In order to increase the efficiency, soft switching is widely used in DC-DC converters. Voltage source converter has high current ripples, while a current source converter requires voltage clamp circuit. The converter is based on dual half bridge topology

compared to the dual full bridge topologies, it has half of the component count for the same rating without additional devices. Without no more devices is added in the unified ZVS is achieved in either direction. It has less control at the mean time less accessory than full bridge competitors. All the above features allow efficient power conversion, easy control, light weight and compact packaging. A 1.65 kw prototype of the converter has been built and successfully used under full power. The experimental results of the converters steady state operation confirms the theoretical analysis and simulation results. It is best alternative for full bridge isolated bidirectional DC – DC converter in high power applications and distinct advantages for high power density and low cost applications.Due to their ability to reverse the direction of flow of current and thereby power, while maintaining the voltage polarity at either end unchanged.

II. CIRCUIT OPERATION & PRINCIPLE

The circuit operates bidirectional DC-DC converter is shown in Fig.1. The circuit operates with dual half bridge placed on each side of the isolation transformer when power flows from the low voltage side to the high voltage side, the circuit works in boost mode. When power flows from the high voltage side to the low voltage side the circuit works in buck mode. A dual half bridge is used instead of dual full bridge at the same output power.

1. The dual half bridge produces the same output power as the dual full bridge.

2. The dual half bridge function uses only half as many devices as the full bridge function.

3. The L.V. Side twice that of the input voltage (12v).The block of fuel cell power bus and energy management system. The low voltage bus is 12V battery and the high voltage bus is the fuel cell voltage is 150V to 300V. The circuit consists of an inductor L_{DC} on the battery side.

Fig. 1 shows block diagram of fuel cell powerbus and energy amanagement system. The low voltage bus is 12V battery and the high voltage bus is the fuel cell voltage 150-300V
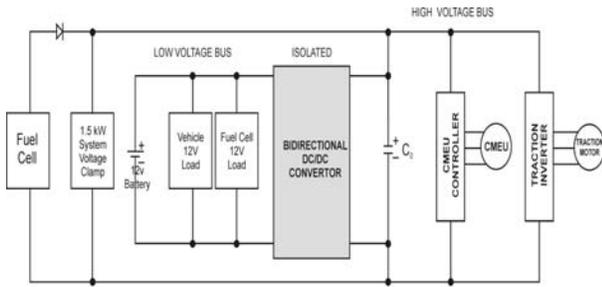
Fig. 1 Block diagram of fuel cell
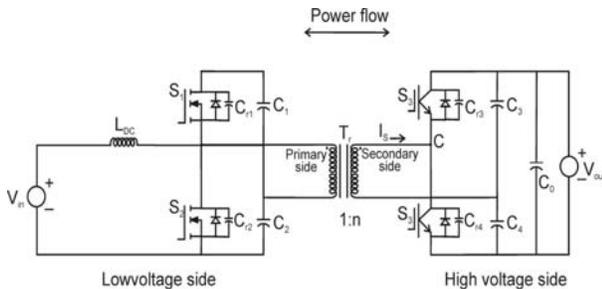
Fig. 2. Soft switched bidirectional half-bridge dc-dc converter

The voltage source is connected in series with the L_{DC} in this form the circuit leads the free from ripple. When the tow switches is provided on either side of the main transformer.

In each switching circuit a small capacitor is connected in parallel to act as a soft switching. When the power flows from low voltage side to high voltage side the circuit works in a boost mode. When the power flows from high voltage side to low voltage side the circuit works in a buck mode.

The converter was developed to improve some characteristic of cuk converter as 1. Isolation, 2. Soft switching, 3. Active voltage clamping.

The leakage inductance of the transformer is utilized as an interface and energy transfer element between the two voltage-source half bridge inverters: LVS and HVS half bridges. Fig. 3 shows the energy transfer principle [4]. The two voltage-source half bridge inverters: LVS and HVS half bridges, each generates a square-wave voltage applied to the primary and secondary of the transformer, respectively. The amount of power transferred is determined by the phase shift of the two square-wave voltages. The current waveform is determined by the phase shift and voltage relationships (V_1 and V_3) and (V_2 and V_4). The optimum case would be ($V_1 = V_3$) and ($V_2 = V_4$). to minimize the peak current. Detailed analysis will be given in Section IV. However, it should be noted here that the two half bridges could have a synchronized duty cycle control rather than 50%. When the duty cycle is 50%, we obtain the easiest and most traditional case of $\phi_2 = \pi$, $V_1 = V_2$ and $V_3 = V_4$. This paper focuses on the 50% duty cycle case
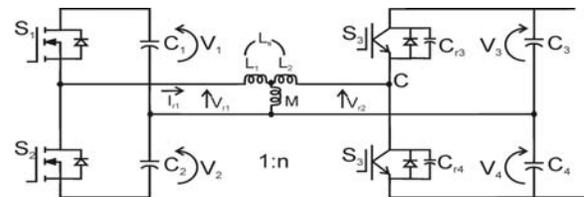
Fig. 3(a) simplified equivalent circuit referred to the primary.

The use of the dual half-bridge topology instead of a dual full-bridge configuration can be justified as follows.

A comparison of total device rating (TDR) in full bridge and half bridge can be made as shown in Fig. 4. The full bridge is used to produce a high-frequency square-wave ($+ V_{DC}$ and $+ V_{DC}$) voltage. Each switching device in the full bridge is subject to a voltage

stress equal to the DC-input voltage V_{DC}, and the current stress is equal to the load current (I_{AC}) .
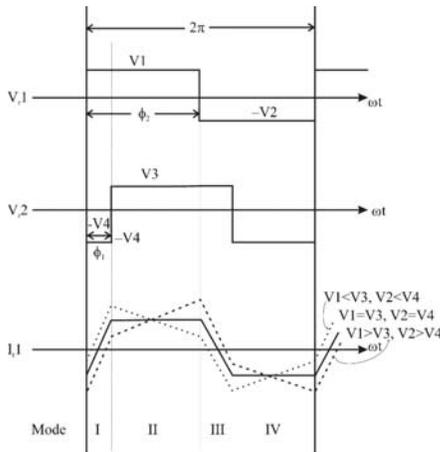
Fig.3b – Idealized voltage and current waveforms of transformer, Note that V_3 and V_4 are the values after referred (a factor of 1/n) to the primary.

The TDR of the full bridge is calculated as $TDR_F = V_{DC}.\ I_{AC}.$ (4 devices) $= 4.P_0$, where P_0 is the output power. The LVS half bridge in the proposed converter (Fig. 2) boosts the DC-rail voltage to twice the DC-input voltage ($2V_{DC}$) and generates a same high-frequency square-wave $(+V_{DC}$ and $-V_{DC})$ voltage with when operated at 50% duty cycle. Therefore, for the half bridge in Fig. 4, each switching device's voltage stress is twice the dc input voltage ($2V_{DC}$) , and the current stress is still the load current (I_{AC}). Similarly, the TDR of the half-bridge can be calculated as $TDR_F = (2V_{DC}).\ I_{AC}.$ (2 devices) $= 4.P_0$, devices , where P_0 is again the output power.

The conclusions can be made as follows.
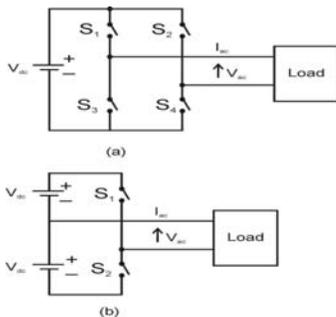
Fig. 4 – comparison of idealized voltage and current waveforms of transformer, Note that V_3 and V_4 are the values after referred (a factor of 1/n) to the primary.

1. The total device rating is the same for the dual half bridge topology and the dual full bridge, for the same output power.

2. Although the devices of the half-bridge are subject to twice the dc input voltage, this is an advantage in EV/HEV and fuel cell applications, because the dc input voltage is very low (12 V battery).

3. The dual half bridge topology uses only half the number of devices as the full-bridge topology.

The major drawback of the half bridge is the split dc capacitors that have to handle the full load current. For the intended application, high current electrolytic capacitors in conjunction with high frequency polypropylene capacitors are used. The other advantages of the proposed circuit are

1. the LVS half bridge produces a relatively ripple-free dc current that is desirable and friendly to the low-voltage source (fuel cell or battery);

2. current ratings (stresses) are minimized for the LVS switching devices and transformer thanks to the boost function of the LVS half bridge;

3. the unified soft-switching capabilities in either direction of power flow without additional switching devices are achieved.

This will be described in the following section. The low input ripple current is achieved due to the current source functionality in this converter. Other topologies (e.g., the full bridge) can also operate as current source. However, a relatively large active clamping circuit is needed for such current source full bridge as indicated in [1], [2].

Step 1	(*before* t_1): Circuit steady state. S1 and D3 are conducting.
Step 2	($t_1 - t_2$): At t_1, S_1 is turned off C_{r1}, C_{r2}. and t_r begin to resonate, making V_{Cr2} across C_{r2} fall from $V_1 + V_2 \cdot V_{r1}$ also drops from V_1. The rate of change depends on the magnitude of, which is the difference between I_{r1} and I_{d1} at t_1.

Step 3	$(t_2 - t_3)$: At t_2, V_{Cl2} attempts to overshoot the negative rail. D_2 is therefore forward biased. During this period, S_2 can be gated on at zero voltage.
Step 4	$(t_3 - t_4)$: From t_3, I_{r1} is less than I_{d1}, so S_2 begins to transfer current from $D_2 \cdot I_{r1}$ keeps on decreasing until it is equal to 0 at t_4. D_3 is thereby still conducting until t_4.
Step 5	$(t_4 - t_5)$: From t_4 to t_5, I_{r1} begins to change polarity; therefore, current is commutated from D_3 to S_3.
Step 6	$(t_5 - t_6)$: At t_5, S_3 is gated to turn off. C_{r3} and C_{r4} begin to be charged and discharged, respectively. The rate of change of the voltage depends on I_{r1} at t_5.
Step 7	$(t_6 - t_7)$: At t_6, when V_{Cr4} attempts to overshoot the negative rail, D_4 is forward biased. During this period, S_4 can be gated on at any time at zero voltage.
Step 8.	$(t_7 - t_8)$: At t_7, S_2 is gated off. C_{r1}, C_{r2} and T_r begin to resonant again, making V_{Cr1} across C_{r1} discharge from $V_1 + V_2 \cdot V_{r1}$ therefore increases from $- V_2$. The rate of change now is decided primarily by the sum of the magnitude of I_{d1} and I_{r1}.
Step 9	$(t_8 - t_9)$: At t_8, when V_{Cr1} attempts to overshoot the positive rail, D_1 is forward biased. I_{r1} increases until it equals 0 at t_9. During this period, S_1 can be gated on at zero voltage.
Step 10	$(t_9 - t_{10})$: From t_9 to t_{10}, I_{r1} begins to change its polarity and continues to increase until it equals I_{d1}. The current is commutated from D_4 to S_4.

Step 11	$(t_{10} - t_{11})$: From t_{10} to t_{11}, I_{r1} begins to exceed I_{d1}. The current is transferred from D_1 to S_1.
Step 12	$(t_{11} - t_{12})$: At t_{11}, S_4 is gated to turn off. C_{r3} and C_{r4} begin to be charged and discharged again. The charge/discharge rate depends mainly on the magnitude of I_{r1} at t_{11}.
Step 13	$(t_{12} - t_{13})$: At t_{12}, when $\{V_{cr3}$ attempts to overshoot the positive rail, D_3 is forward biased. The circuit returns to the original steady state. During this period

Commutation in the proposed circuit is similar to the diode-to-switch commutation mode of the ARCP inverter [14], i.e., turn-off of the main conducting device diverts the current to the corresponding resonant capacitors to charge one and discharge the other, resulting in a zero voltage turn-off. The zero voltage turn-on is achieved by gating on the in-coming device while the anti-parallel diode is conducting. However, unlike ARCP inverter, the proposed circuit does not require an auxiliary circuit to achieve soft switching. From Fig. 6, it is clear that the conditions of soft switching in boost mode depend on the magnitude of I_{r1} and I_{d1} at t_1, t_5, t_7 and t_{11}, respectively. This is summarized as

$$\left\{ \begin{array}{l} I_{r1}(t_1) > I_{d1}(t_1) \qquad \qquad ...(1) \\ I_{r1}(t_5) < 0 \\ I_{r1}(t_7) > I_{d1}(t_7) \\ I_{r1}(t_{11}) > 0 \end{array} \right.$$

A. Boost Mode

It is observed that the rate of change of the voltage of S_1 and S_2 at t_1 is different from that of t_7. This is because the turn-off currents are different at their switching instants. Similarly, devices S_3 and S_4 have different voltage change rates at t_5 and t_7. Comparing these four voltage slopes, dv/dt at t_1 and dv/dt at t_7 represents the minimum and maximum, respectively, because the turn-off current is minimum at t_1 and maximum at t_7. As a result, the allowable minimum and maximum dv/dt should be designed according to the application requirements.

B. Buck Mode

Because of the half-bridge topology of the two sides is symmetrical, the operation principles in buck mode are similar to those in boost mode. Fig. 8 describes one switching cycle in buck mode. Due to the reversed power-flow direction, the phase of V_{r2} is leading V_{r1}. In addition, the inductor current I_{d1} is reversed. The buck mode operation can also be divided into thirteen steps. The description of each step can be analogously inferred and will not be discussed here.

Like boost mode, the soft-switching conditions in buck mode can be derived similarly as

$$\left\{ \begin{array}{l} I_{r1}(t_1) < 0 \\ I_{r1}(t_5) > I_{d1}(t_5) \\ I_{r1}(t_7) > 0 \\ I_{r1}(t_{11}) < I_{d1}(t_{11}) \end{array} \right. \quad ...(2)$$

Software Program (Boost Mode)

```
ORG 00H
MOV P1, # 00H
MOV P3, # OFFH
MOV A, # 00H
START: MOV A, P3
ANL A, # 01H
JZ BOOST
MOV P1, # 05
CALL DELAY
MOV P1 , # OAH
CALL DELAY
SJMP START
BOOST: MOV P1, # 50H |
CALL DELAY
MOV P1, #0A 0H
CALL DELAY
SJMP START
DELAY: MOV R1, # 25H
LOOP: NOP
DJNZ R1, LOOP
ret
```
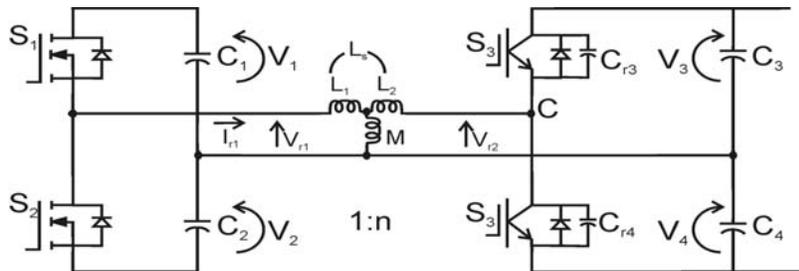

Fig. 5. Wave forms and switching primary referred equivalent circuit.
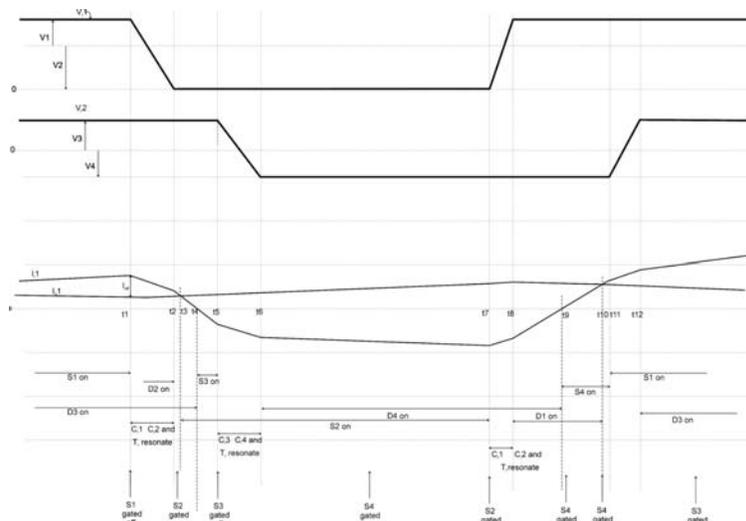
Fig. 6. Wave froms and switching timing of boost mode
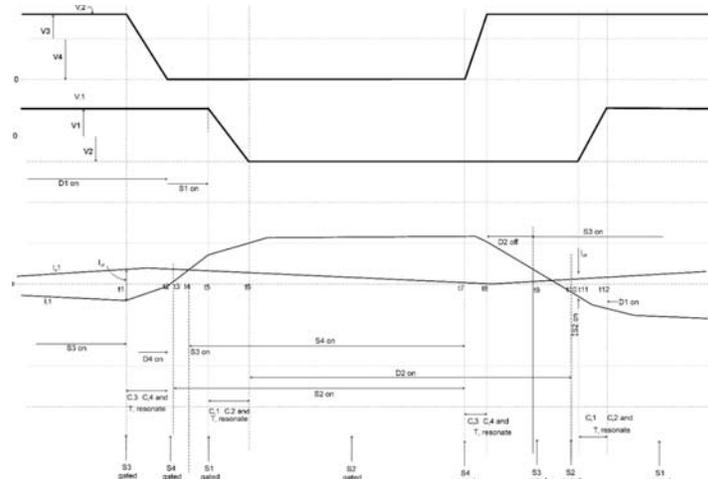
Fig. 7. Wave forms and switching timing of buck mode

Mathematical Analysis of circuits

This section deals with the calculations of DC-DC converter of ZVS and ZCS. The calculation used to find out the output voltage control region of the converters. The formula is utilized to be calculated the output voltage. $n = N_1/N_2$

$n =$ turn ratio of transformer

switching frequency $f_s = 1/T$ angular switching frequency, $\omega_s = 2\pi f_s$

$$V_0 = V_{in}/D.$$

III. SIMULATION VERIFICATION

DC to DC converter operating in boost mode is shown in Fig 8(a). The scopes are connected to display the driving pulses, primary voltage, secondary voltage and DC output voltage. DC input voltage is applied to the bidirectional DC to DC converter operating in boost mode is shown in Fig 8(b).

Driving pulses applied to the MOSFET M1 and M2 as shown in Fig 8(c). Voltage across the primary is shown in Fig 8(d). This stepped up using a step upto 230 volt as shown in Fig 8(e). DC output voltage is shown in Fig 8(f).

The current through the transformer is shown in Fig 8(g) and boost mode DC output current is shown in Fig 8(h). The graph is plotted between the input Vs output power is shown in Fig 8(i).

Bidirectional converter is operating in buck mode is shown in Fig 9(a). DC is converted into AC by using the full bridge inverter on the output side is stepped down and converted into DC by using a diode rectifier. The DC input voltage is shown in Fig 9(b). The inverter output

voltage is shown in Fig 9(c). Output voltage is shown in Fig 9(d) and the buck mode DC output current is shown in Fig 9(e). Thus DC to DC converter is capable of transferring power in either Direction. The graph is plotted between the input Vs output power is shown in Fig 9(f).
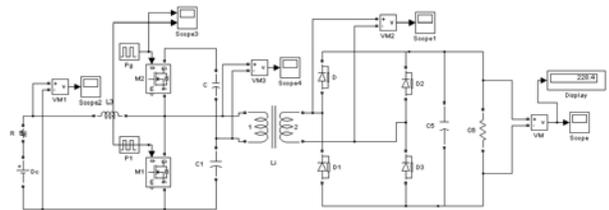
Fig. 8(a) Boost mode circuit diagram
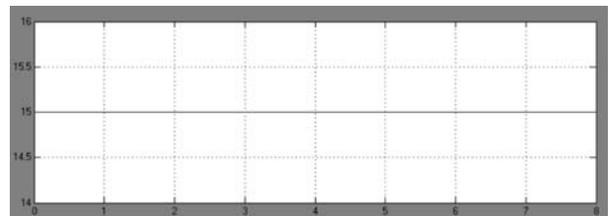
Fig. 8(b) DC Input voltage
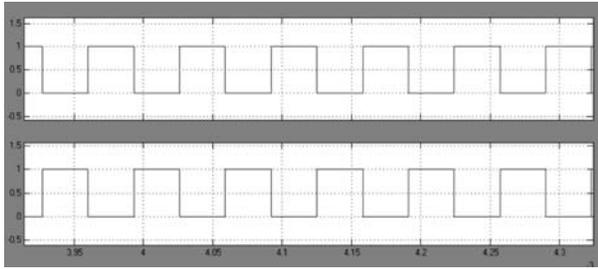
Fig. 8(c) Driving pulses
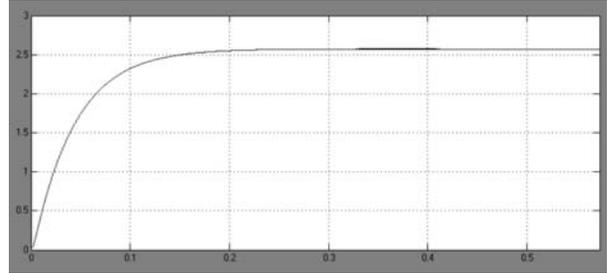
Fig. 8(h) DC output current
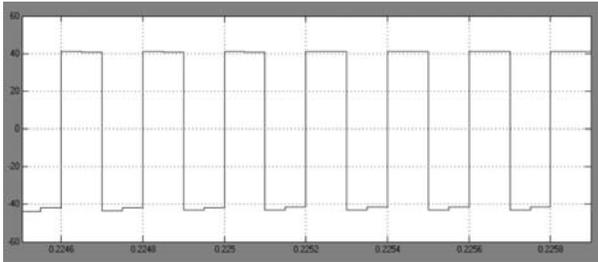
Fig. 8(d) Transformer primary side voltage
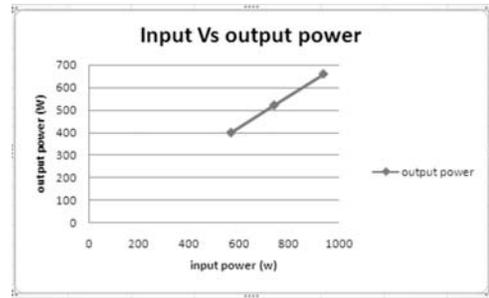
Fig. 8(i) DC input Vs output power
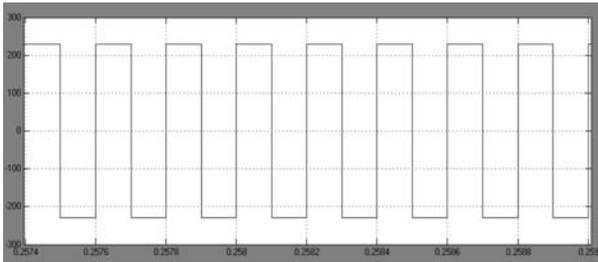
Fig. 8(e) Transformer secondary side voltage
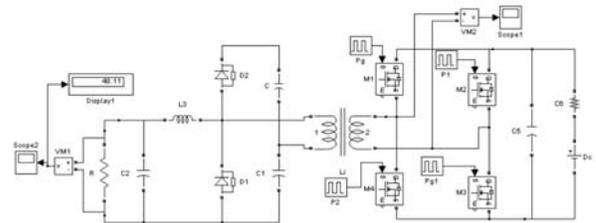
Fig. 9(a) Buck mode circuit diagram
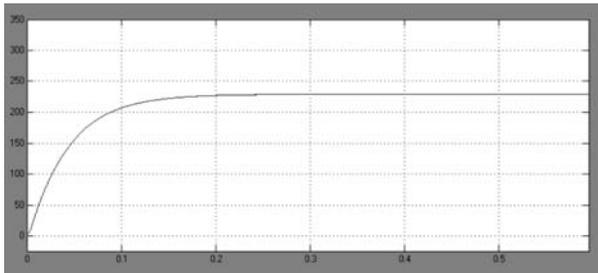
Fig. 8(f) Boost mode DC output voltage
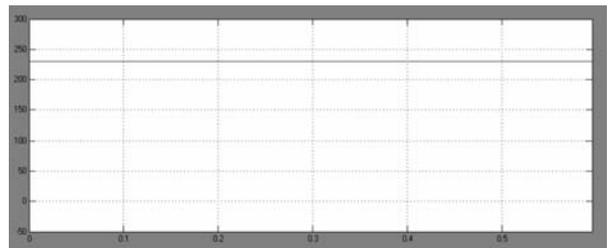
Fig. 9(b) DC input voltage
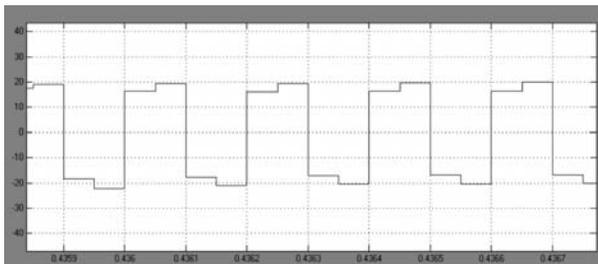
Fig. 8(g) Current through transformer
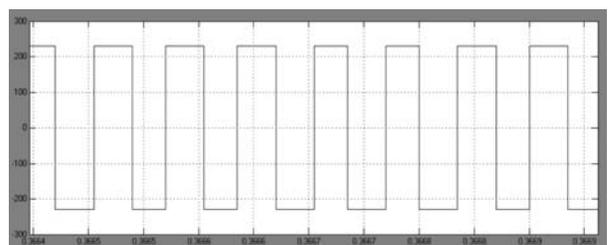
Fig. 9(c) Inverter output
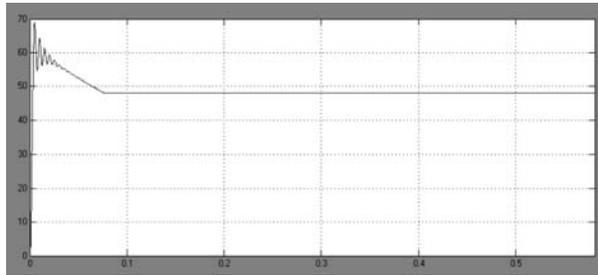
Fig. 9(d) DC output voltage
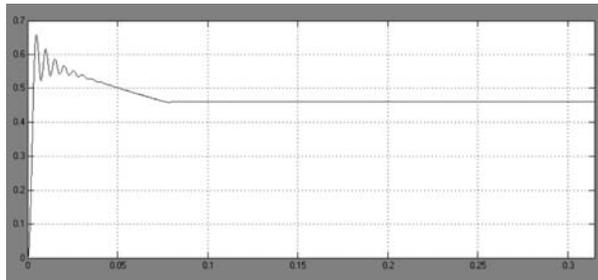
Fig. 9(e) DC output current
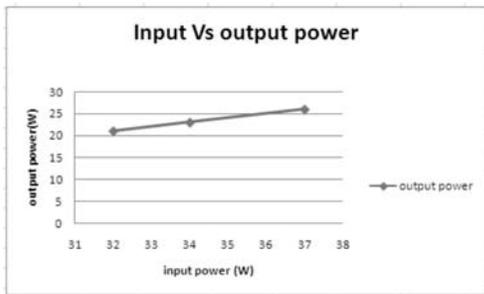
Fig. 9(f) DC input Vs output power

IV. EXPERIMENTAL VERIFICATION

Laboratory model of bidirectional DC to DC converter is fabricated and tested in the laboratory. Driving pulses required by the MOSFET are generated using 89C51. They are amplified by using driver amplifier. Top view of the hardware is shown in Fig 10(a). The hardware consist of power supply board, driver board and transformer board. The input DC voltage is 24 V as shown in Fig 10(b). Driving pulses are shown in Fig 10(c). The inverter output voltage is shown in Fig 10(d). The boost output voltage is shown in Fig 10(e). The buck output voltage is shown in Fig 10(f).
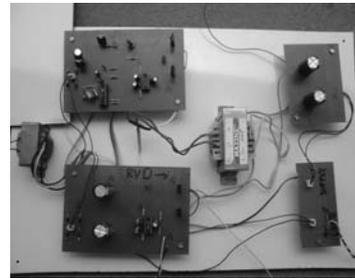
Fig. 10(a) Hardware layout
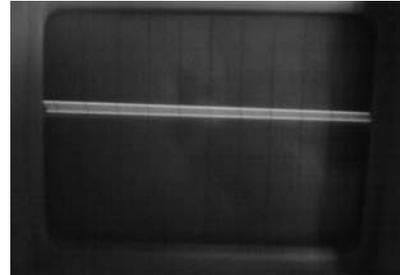
Fig. 10(b) DC input voltage
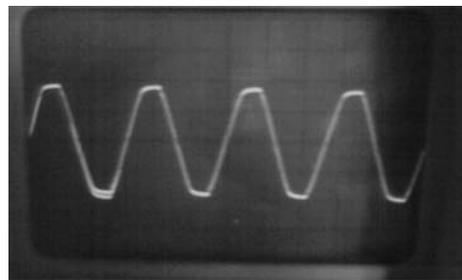
Fig. 10(c) AC input voltage
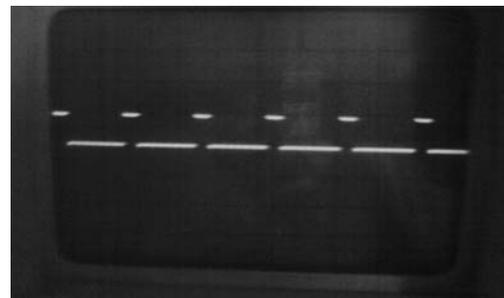
Fig. 10(d) Driving pulses
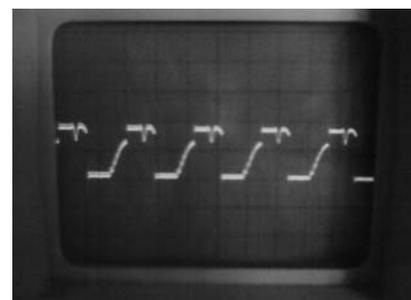
Fig. 10(e) Inverter output voltage
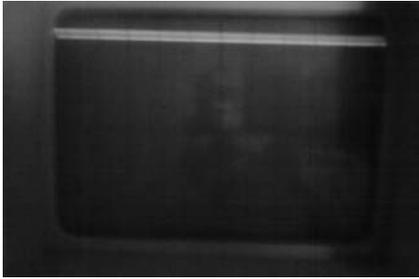
Fig. 10(f) Boost output voltage
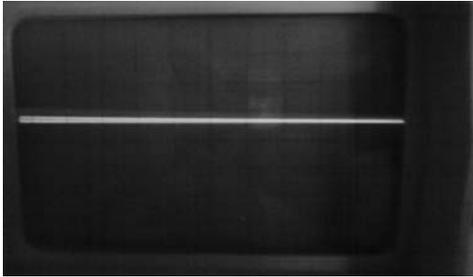
Fig. 10(g) Buck output voltage

V. CONCLUSION

This paper presents a soft switched bidirectional DC-DC converter compared with the other bidirectional DC-DC converters. The performance is excellent compared with the full bridge the same output is produced also with the higher efficiency. The total number of components is reduced unidirectional soft switching scheme is achieved without any auxiliary circuit. ZVS is applied in all switches of the device in either direction of power flow. It has low cost, modified design light weight, compact and reliable. The simulation and experimental results are presented. The experimental results are closely agree with the simulation result.

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